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Description

FAST DIGITAL DATA RECOVERY CIRCUIT

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a digital data recovery circuit, and more particularly, to a digital data recovery circuit using a phase-detecting, level-determining device to detect the phase, and thereby to determine a reference level signal.

[0003] 2. Description of the Prior Art

[0004] Digital data recovery circuit, which compares an analog input signal with a reference level signal to determine whether the binary value of the input signal represents "0" or "1", i.e. to convert the analog input signal into a digital output signal, are widely used in transmission systems.

[0005] Please refer to Fig.1 showing a block diagram of a conventional digital data recovery circuit 100. The digital data recovery circuit 100 has a comparator 120 and a low pass filter 140. The Xi1 is the signal input into the digital data recovery circuit 100. The comparator 120 compares the

input signal Xi1 with a reference level signal Vc1 and outputs a sliced signal Xo1. The sliced signal Xo1 will be of a first binary value when the level of Xi1 is lower than the level of Vc1, and of a second binary value when the level of Xi1 is higher than the level of Vc1. As an example, the first binary value is "0" and the second binary value is "1." In this case, that Xo1 is at "1" represents the input signal Xi1 has a higher level than Vc1, while that Xo1 is at "0" represents the input signal Xi1 has a lower level than Vc1.

[0006] Since the input signal Xi1 contains a direct current (DC) component, which usually varies in accordance with time, the reference level signal Vc1 must be able to be adapted to trace the DC component of the input signal Xi1 so that the comparator 120 can slice Xi1 into Xo1 correctly. In other words, Vc1 should be kept equivalent to the DC component of Xi1.

[0007] Therefore, in the prior art, the sliced signal Xo1 passes through the low pass filter 140 to generate the reference level signal Vc1 to be used as a feedback signal. After being processed by the low pass filter 140, Vc1 will gradually approach the DC component of Xi1. And when the DC component of Xi1 varies, Vc1 will vary accordingly. The closer Vc1 is to Xi1, the more accurately Xo1 represents

the "0"/"1" inside the input signal Xil.

[0008] Please refer to Fig.2 showing a block diagram of another conventional digital data recovery circuit 200. The digital data recovery circuit 200 includes a comparator 220, an up/down counter (UDC) 240, and a digital-to-analog converter (DAC) 260. The Xi2 is the signal input into the digital data recovery circuit 200. The comparator 220 compares the input signal Xi2 with a reference level signal Vc2 and outputs a sliced signal Xo2. The sliced signal Xo2 will be of a first binary value when the level of Xi2 is lower than the level of Vc2, and of a second binary value when the level of Xi2 is higher than the level of Vc2.

[0009] Without loss of generality, assume that the first binary value is "0" and the second binary value is "1". In the case of the sliced signal Xo2 being "0", whenever a clock K2 transits upwards (from "0" to "1"), the counter value DL2 output by the UDC 240 is decreased by one. In the case of the sliced signal Xo2 being "1", whenever a clock K2 transits upwards, the counter value DL2 output by the UDC 240 is increased by one. In a result, the reference level signal Vc2 output by the DAC 260 will gradually approach a DC component of Xi2. And when the DC component of Xi2 varies, Vc2 will be adapted to trace the variation of

Xi2. The closer Vc2 is to Xi2, the more accurately the sliced signal Xo2 generated by the comparator 220 represents Xi2.

[0010] The problem of the prior art is that the reference level signal requires a specific amount time to approach the DC component of the input signal, meaning that before the approach, the sliced signal output by the comparator may not effectively represent the binary values of the input signals.

[0011] Briefly, the digital data recovery circuit in the prior art requires a specific approach time to allow the reference level signal to approach the DC component of the input signal, in order to have the sliced signal represent the binary value of the input signals accurately.

SUMMARY OF INVENTION

[0012] It is therefore a primary objective of the claimed invention to provide a digital data recovery circuit capable of adjusting a reference level signal to approach a DC component of an input signal, in order to solve the problem mentioned above.

[0013] Briefly, a digital data recovery circuit for converting an input signal into a sliced signal includes a comparing device coupled with the input signal and a reference level signal

for comparing the input signal with the reference level signal and generating the sliced signal according to the result of comparison, a phase-detecting, level-determining device coupled with the comparing device for detecting the phase at which the transition of the sliced signal occurs, based on a reference clock, and generating a digital level signal according to the result of detection, and a digital-to-analog converter (DAC) coupled with the phase-detecting, level-determining device for generating the reference level signal for the comparing device according to the digital level signal.

[0014] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0015] Fig.1 is a block diagram of a conventional digital data recovery circuit.

[0016] Fig.2 is a block diagram of another conventional digital data recovery circuit.

[0017] Fig.3 is a block diagram of a digital data recovery circuit according to the present invention.

[0018] Fig.4 is a timing diagram of the system in Fig.3.

[0019] Fig.5 is a circuit diagram of the phase detector.

[0020] Fig.6 is a timing diagram of each clock and sliced signal.

[0021] Fig.7 is a circuit diagram of the transition phase detecting device.

Detailed Description

[0022] Please refer to Fig.3 showing a block diagram of a digital data recovery circuit 300 according to the present invention, which converts an analog input signal Xi3 into a digital sliced signal Xo3. The data recovery circuit 300 includes a comparing device 320 coupled with the input signal Xi3 and a reference level signal Vc3 for comparing Xi3 with Vc3 to generate the sliced signal Xo3, a phase-detecting, level-determining device 340 coupled with the comparing device 320 for detecting the phase at which the transition of Xo3 occurs, according to a reference clock CLK (not shown in Fig.3. The frequency of CLK is equal to the bit rate of Xi3.), and thereby generating a corresponding digital level signal DL3, and a DAC 360 coupled with the phase-detecting level-determining device 340 and the comparing device 320 for generating the reference level signal Vc3 according to the digital level

signal DL3 for the comparing device 320. Please notice that the digital sliced signal Xo3 generated by the comparing device 320 can be a single bit or a plurality of bits. For a clearer description, a single bit Xo3 is described in the followings.

[0023] In the case of the level of the input signal Xi3 being lower than the level of the reference level signal Vc3, the sliced signal Xo3 output by the comparing device has a first binary value, and in the case of the level of the input signal Xi3 being higher than the level of the reference level signal Vc3, the sliced signal Xo3 output by the comparing device 320 has a second binary value. For a clearer description, assume that the first binary value is "0" and the second binary value is "1." Physically, the value "0" of Xo3 corresponds to a first voltage level V1; while the value "1" corresponds to a second voltage level V2, and V2>V1. Please notice that the comparing device can be a comparator, a one-bit analog-to-digital converter (ADC), a multi-bit ADC or a partial-response maximum likelihood circuit.

[0024] The sliced signal Xo3 output by the comparing device 320 is a square wave switching between the first level V1 and the second level V2. The closer the level of the reference

level signal Vc3 is to a DC component of the input signal Xi3, the more accurately Xo3 represents a signal component of Xi3. In order to achieve to goal, the phase-detecting, level-determining device 340 and the DAC 360 must cooperate with each other to generate an accurate reference level signal Vc3 for the comparing device 320.

[0025] Please refer to Fig.4 showing a timing diagram, as an example, of the system in Fig.3. The period of the reference clock signal CLK has been configured in advance to match the duration of the data bits carried by Xo3. In this diagram, the level of the reference level signal Vc3 is initially lower than the DC component of the input signal Xi3; thus the duty cycle of the sliced signal Xo3 output by the comparing device 320 is higher than 50%, i.e. the period during which Xo3 is kept at the first level V1 is shorter than the period of the reference clock CLK, or in other words, the period during which Xo3 is kept at the second level V2 is longer than the period of the reference clock signal CLK.

[0026] The situation that the duty cycle of the sliced signal Xo3 is larger or less than 50% can be realized by examining the transitions of Xo3. For instance in Fig.4, based on the reference clock CLK, Xo3 transits at PHASE 1, which is 340°

as shown in Fig. 4, from the second level V2 to the first level V1, then transits at PHASE 2, which is 230° as shown in Fig. 4, from the first level V1 to the second level V2, and then transits at PHASE 3, which is 340° as shown in Fig. 4, from the second level V2 to the first level V1. Note that all the phase mentioned here is a phase value related to the reference clock signal CLK, and the phase recurs once every 360 degrees, thus the phase over 360 degrees must be converted between 0 degree and 360 degrees. It is observed that since the period during which Xo3 is kept at V1 will be less than the period of the reference clock CLK (or less than n times the period of the reference clock CLK, wherein n is an integer), PHASE 2 - PHASE 1 is a negative value (e.g. PHASE 2 - PHASE 1 = -110°). It is observed that since the period during which Xo3 is kept at V2 is longer than the period of the reference clock CLK (or more than n times the period of the reference clock CLK, wherein n is an integer), PHASE 3-PHASE 2 is a positive value (e.g. PHASE 2 - PHASE 1 = 110°).

[0027] In result, based on the reference clock CLK whose frequency is the same as the bit rate of the input signal Xi3, by detecting the phase during the transition of the sliced signal Xo3, the duty cycle of Xo3 can be known. If the

duty cycle is higher than 50%, the level of the reference level signal Vc3 should be raised, and if the duty cycle is lower than 50%, the level of the reference level signal Vc3 should be lowered down.

[0028] As shown in Fig.3, the phase-detecting, level-determining device 340 includes a phase detector 370 coupled with the comparing device 320 for detecting the phase at which the sliced signal Xo3 transits from the first binary value to the second binary value (i.e. the level transits from the first level V1 to the second level V2), and detecting the phase at which the sliced signal Xo3 transits from the second binary value to the first binary value (i.e. the level transits from the second level V2 to the first level V1), based on the reference clock CLK, and a level determiner 390 coupled with the phase detector for generating digital level signals DL3 corresponding to the result of detection.

[0029] Please refer to Fig.5 showing a circuit diagram of the phase detector 370. Some symbols are introduced here: N is a predetermined positive integer, K is a positive integer between 1 and N, and L is a positive integer between 1 and N-1. The phase detector 370 includes N number of delay flip-flop series (D flip-flop series) 510 and N num-

ber of transition phase detecting devices 530. Each D flip-flop series 510 has an input end, a clock input end, and an output end. The input end of each D flip-flop series 510 is coupled with the sliced signal Xo3, and the clock input end of the K^{th} D flip-flop series 510 is coupled with a clock signal CLK_K generated by delaying the reference clock CLK for K/N period. Each transition phase detecting device 530 has a first input end, a second input end, a first output end, and a second output end. The first input end of the L^{th} transition phase detecting device 530 is coupled with the output end of the L^{th} D flip-flop series 510, and the second input end is coupled with the output end of the $L+1^{th}$ D flip-flop series 510. The first input end of the N^{th} transition phase detecting device 530 is coupled with the output end of the N^{th} D flip-flop series 510, and the second input end is coupled with the output end of the 1^{st} D flip-flop series 510.

[0030] Please notice that in the present embodiment, each D flip-flop series 510 has two D flip-flops 511; however, the use of one or more than one D flip-flop 511 are also covered by the present invention. The reason for using more than one flip-flop is to ensure signals output by the D flip-flop series 510 are accurate (Metastability can be prevented by

using two flip-flops. Metastability occurs when the transition edge and the clock edge of Xo3 are too close to each other. Once metastability occurs, the Q value of the flip-flop may be unstable; this problem can be simply solved by cascading more than one flip-flop). Based on the reference clock CLK, the phase of CLK_K is K/N (in this case the phase is represented by the period; it will be 360 * K/N when represented by degree), thus CLK_N is just the reference clock CLK itself (thus no need to be delayed).

[0031] For a clearer description of the phase detector 370 in Fig.5, please refer to Fig.6 showing a timing diagram of each clock CLK_K, K=1,...,N and an exemplary sliced signal Xo3 in the case of N=6. Note that the clock CLK_K represents just the original reference clock. That N=6 implies that the period T of the clock CLK is equally divided into 6 sub-periods, as shown in the Fig. 6. Taking the beginning time of the period as a reference, the sub-periods start at time points of 0, 1/6, 2/6, 3/6, 4/6, 5/6, respectively. Notably, these time points have been normalized by T for clear notation. Since each of these time points can also be used or represent the phase at which the corresponding sub-period falls. In the following, we will express the phase in this way. Suppose the level of the ref-

erence level signal Vc3 is higher than the DC component of the input signal Xi3, the time duration during which Xo3 is kept at the second level (i.e. "1") would be less than the period of the reference clock CLK. Taking the CLK as a reference, suppose that the phase at which Xo3 transits upwards (from "0" to "1") falls between 1/6 and 2/6, and the phase at which Xo3 transits downwards (from "1" to "0") falls between 0 (i.e. 6/6) and 1/6. As well known, in the operation of the flip-flops 511, the signal from the input end will be transmitted to the output end only when signal at the clock input end transits from "0" to "1". Therefore, the output end of the second D flip-flop series 510 will become "1" firstly, and the output ends of the third, fourth, fifth, and sixth D flip-flop series 510 will also become "1" in sequence. On the other hand, since Xo3 transits downwards between phase 0 and 1/6, the output end of the first D flip-flop series 510 will become "0" firstly, and the output ends of the second, third, fourth, and fifth D flip-flop series 510 will become "0" in sequence. Actually, since the phase of the sliced signal Xo3 is between 1/6 and 2/6 in upward transition, the output ends of the second, third, fourth, fifth, and sixth D flip-flop series 510 becomes "1" in sequence, and since

the phase of the sliced signal Xo3 is between 0 and 1/6 in downward transition, the output ends of the second, third, fourth, and fifth D flip-flop series 510 becomes "0" in sequence. In result, the output of each D flip-flop series 510 will extract the signal level of the sliced signal Xo3 at specified phase. Therefore, having the output results of the D flip-flop series 510, it is enough to tell which sub-period the transition of the sliced signal Xo3 occurs at. Accordingly, the value of the digital level signal DL3 can be determined, as will be shown later.

[0032] A plurality of transition phase detecting devices are employed to detect the phase at which the phase transition of the sliced signal Xo3 occurs, based on the output results of the N number of D flip-flop series. Let R be an integer between 1 an N. An R^{th} transition phase detecting device 530 includes an upward transition detecting unit 531 and a downward transition detecting unit 532. The upward transition detecting unit 531 has a first input end coupled with a first input end of the R^{th} transition phase detecting device 530, a second input end coupled with a second input end of the R^{th} transition phase detecting device 530, and an output end used as a first output end of the R^{th} transition phase detecting device 530.The down-

ward transition detecting unit 532 has a first input end coupled with the first input end of the R^{th} transition phase detecting device 530, a second input end coupled with the second input end of the R^{th} transition phase detecting device 530, and an output end used as a second output end of the R^{th} transition phase detecting device 530.

[0033] Based on the block diagrams of the transition phase detecting devices 530 shown in Fig. 5, it can be found that either when the first and second input values are both "0" or "1", the first and second output values will be "0". Moreover, when the first input value is "0" and the second input value is "1", the first output value will be "1" and the second output value will be "0." And, when the first input value is "1" and the second input value is "0", the first output value will be "0" and the second output value will be "1". In such a way, the upward transition detecting unit 531 is capable of detecting the upward transition of the sliced signal Xo3, and the downward transition detecting unit 532 is capable of detecting the downward transition of the sliced signal Xo3. Now please refer again the example shown in Fig.6. Initially, the outputs of each D flip-flop series 510 are set to be "0". During the period P_A, the sixth D flip-flop series 510 will be triggered by the clock

CLK_6 and latch the signal level, which is "0" in the example, of the sliced signal Xo3 at the starting time instant of the period P_A. The outputs of the other D flip-flop series 510 will remain since their associated clock signals does not trigger them to update their outputs. During the period P_B, the first D flip-flop series 510 will be triggered by the clock CLK_1 and latch the signal level, which is "0" in the example, of the sliced signal Xo3 at the starting time instant of the period P_B. Similarly, during the period P_C, the second D flip-flop series 510 will output "1". As can be seen, the output "0" of the first D flip-flop series 510 and the output "1" of the second D flip-flop series 510 will remain during the next periods P_D, P_E, and P_F.

[0034] On the other hand, during the period P_G, the sixth D flip-flop series 510 will be triggered by the clock CLK_6 and latch the signal level, which is "1" in the example, of the sliced signal Xo3 at the starting time instant of the period P_G. The outputs of the other D flip-flop series 510 will remain since their associated clock signals does not trigger them to update their outputs. During the period P_H, the first D flip-flop series 510 will be triggered by the clock CLK_1 and latch the signal level, which is "0" in the example, of the sliced signal Xo3 at the starting time instant of

the period P_H. As can be seen, the output "1" of the sixth D flip-flop series 510 and the output "0" of the first D flip-flop series 510 will remain during the next periods P_I, P_J, and P_K.

[0035] Let A and B are both positive integers between 1 and N. Generally speaking, when the Xo3 transits from "0" to "1" at a phase between (A-1)/N and A/N, the upward transition detecting unit 531 of the A^{th} transition phase detecting device 530 will have its output to be "1" for a period longer than 1.T/N, where T is the period of the reference clock CLK. Note that it is a transient phenomenon and will not be regarded as an actual phase transition event if the output "1" of the transition phase detecting device 530 merely appears during a period of 1.T/N. On the other hand, when the Xo3 transits from "1" to "0" at a phase between (B-1)/N and B/N, the downward transition detecting unit 532 of the B^{th} transition phase detecting device 530 will have its output to be "1" for a period longer than 1.T/N.

[0036] The upward transition detecting unit 531 and the downward transition detecting unit 532 in Fig.5 are both composed of an inverter and an AND gate; however, another composition is possible. Please refer to Fig.7 showing a

circuit diagram of another embodiment of the transition phase detecting device 530. The upward transition detecting unit 531 and the downward transition detecting unit 532 in Fig.7 are composed of an inverter and an OR gate, which is well known by the person skilled in the art to recognize that the transition phase detecting devices 530 shown in Fig. 5 and Fig. 6 perform the identical function, and thus a further description is hereby omitted. Furthermore, it is also obvious that the upward transition detecting units 531 (the downward transition detecting units 532) shown in Fig. 5 and Fig. 7 are equivalent to each other and therefore exchangeable for implementation.

[0037] In the embodiment mentioned above, if the value of the reference level signal Vc3 is accurate, the phase of the sliced signal Xo3 in downward transition differs from that in upward transition for n periods, wherein n is an integer, i.e. the remainder of the two phases is 0. However in this embodiment, the phase of Xo3 in upward transition is detected by the phase detector 370 to be between 1/6 and 2/6, while that in downward transition is between 0 and 1/16, i.e. the remainder of the phase in downward transition minus that in upward transition is negative (0-1/6 or

1/6-2/6). The result of detection shows the time Xo3 is kept at the second level V2 is shorter, i.e. the level of the reference level signal Vc3 is higher than the DC component of the input signal Xi3, so that the level of Vc3 should be adjusted to a lower level. If the remainder of the phase in downward transition minus that in upward transition is positive, the result of detection shows the time Xo3 kept at the first level V1 is shorter, i.e. the level of the reference level signal Vc3 is lower than the DC component of the input signal Xi3, so that the level of Vc3 should be adjusted to a higher level. Of course, the remainder of the phase in upward transition minus that in downward transition can be also used for the adjustment. If the remainder of the phase in upward transition minus that in downward transition is positive, the level of Vc3 should be adjusted to a lower level, and if the remainder of the phase in upward transition minus that in downward transition is negative, the level of Vc3 should be adjusted to a higher level. Of course, the larger the number N in the D flip-flop series 510 and transition phase detecting devices 530, the more accurate the transition phase detected by the phase detector 370.

[0038] After the phase detector 370 in Fig.3 detects the transi-

tion phase of the sliced signal, the level determiner 390 can determine the value of the digital level signal according to the result of detection. Generally, when the result of detection shows the level of the reference level signal Vc3 is lower, the level determiner 390 outputs a higher digital level signal DL3, and when the result of detection shows the level of the reference level signal Vc3 is higher, the level determiner 390 outputs a lower digital level signal DL3. The level determiner 390 can optimize DL3, e.g. if the remainder of the phase in downward transition minus that in upward transition is 3/N, subtract 5 from DL3; if the remainder of the phase in downward transition minus that in upward transition is +1/N, add 2 to DL3. Of course, the more accurate the parameters of the design, the more accurate the system and the more rapidly Vc3 approaches to the DC component of the input signal Xi3.

[0039] Another approach for adjusting the digital level signal DL3 is disclosed as follows. If the phase of the downward transition minus that of the upward transition is negative, the level determiner 390 decrease DL3 by a predetermined amount. On the other hand, if the phase of the downward transition minus that of the upward transition is positive, the level determiner 390 increases DL3 by a predeter-

mined amount. However, in such kind of approach, the level of the reference level signal Vc cannot trace the DC component of the input signal Xi3 very rapidly.

[0040] Following the operations mentioned above, a proper digital level signal DL3 is determined under the cooperation of the phase detector 370 and the level determiner 390.The DAC 360 then converts DL3 into the reference level signal Vc3 so that the comparing device 320 can slice the signal component in the input signal Xi3 accordingly.

[0041] Please notice that in addition to the phase detector 370 being composed of logic gates in Fig.5, the phase detector 370 in Fig.3 can be also composed of a delay lock loop (DLL). Also, the DAC 360 in Fig.3 can be a voltage source for generating the reference level signal Vc3, a current source generating current signals to be converted into Vc3 by an external circuit, or a control circuit for directly controlling the bit value of the sliced signal Xo3 output by the comparing device 320.

[0042] In contrast to the prior art, the digital data recovery circuit according to the present invention determines how to adjust the level of the reference level signal by detecting the phase so that the reference level signal can approach to

the DC component of the input signal rapidly.

[0043] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.